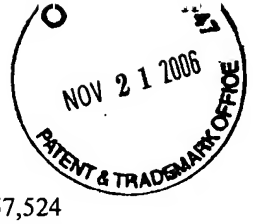


REMARKS/ARGUMENTS

Claims 1-26 have been allowed. New claims 27-54 are added. New claims 27-54 are fully supported by the specification, as described in detail in the section below. Also, Applicants direct the Examiner's attention to the references cited in the Information Disclosure Statement filed concurrently with the present Request for Continued Examination.

Support for Claims 27-54

New claims 27-54 are fully supported by the present specification. Support for specific claim elements is identified below by citing to the present specification as published (United States Patent Publication Number US2004/0205323).

Regarding claim 27, the recited programmable processor comprising in part "an instruction path; a data path; a plurality of registers operable to receive and store data from the data path and communicate the stored data to the data path; and an execution unit coupled to the instruction path and the data path and operable to decode and execute instructions received from the instruction path" is described at Figure 1 and paragraphs 0078-0079.

Regarding claim 27, the recited programmable processor further comprising in part an execution unit "wherein in response to decoding a single instruction specifying a plurality of registers storing a plurality of 8-bit data elements, an index register storing an index vector comprising a plurality of equal-sized selectors stored in partitioned fields of the index register and a destination register, the execution unit is operable to, for each selector in the index vector, provide a data element selected by the selector to a predetermined position in the destination register" is described at Figures 1, 47D, and 47E, and paragraphs 0078-0079, 0081, and 0297.

Regarding claim 28, the recited claim feature "wherein the plurality of registers comprises two registers" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 29, the recited claim feature "wherein the plurality of registers comprises two 64-bit registers storing a combined total of sixteen 8-bit data elements" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 30, the recited claim feature "wherein the number of selectors stored in the index register is equal to the number of predetermined positions in the destination register" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 31, the recited claim feature "wherein the index register is a 64-bit register" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 32, the recited claim feature "wherein the index vector comprises n equal-sized selectors and the destination register comprises n equal-sized predetermined positions" is described at Figures 47D and 47E, and paragraphs 0297.

Regarding claim 33, the recited claim feature "wherein the selector stored in a lowest order set of bits of the index register provides a data element to a lowest order set of bits of the destination register, the selector in a second lowest order set of bits of the index register provide a data element to a second lowest order set of bits of the destination register and the selector stored in a highest order set of bits of the index register provides a data element to a highest order set of bits of the destination register" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 34, the recited claim feature "wherein the destination register is a 128-bit register" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 35, the recited claim feature "wherein each of the equal-sized selectors stored in partitioned fields of the index register is a 4-bit selector" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 36, the recited claim feature "wherein the index register stores sixteen 4-bit selectors" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 37, the recited programmable processor comprising in part "an instruction path; a data path; an external interface operable to receive data from an external source and communicate the received data over the data path; a cache operable to retain data communicated between the external interface and the data path; a plurality of registers operable to receive and store data from the data path and communicate the stored data to the data path; and an execution unit coupled to the instruction path and the data path and operable to decode

and execute instructions received from the instruction path" is described at Figure 1 and paragraphs 0078-0079.

Regarding claim 37, the recited programmable processor comprising in part an execution unit "wherein in response to decoding a single instruction specifying a first register storing a first plurality of 8-bit data elements, a second register storing a second plurality of 8-bit data elements, an index register storing an index vector comprising a plurality of equal-sized selectors stored in partitioned fields of the index register and a destination register, the execution unit is operable to, for each selector in the index vector, provide a data element from one of the first or second plurality of 8-bit data elements selected by the selector to a predetermined 8-bit position in the destination register, wherein the predetermined positions are contiguous blocks of bits that take up an entire width of the destination register" is described at Figures 1, 47D, and 47E, and paragraphs 0078-0079, 0081, and 0297.

Regarding claim 38, the recited claim feature "wherein the first and second registers are 64-bit registers, the index register is a 64-bit register and each selector stored in the index register has a sufficient number of bits to select anyone of the 8-bit data elements in the first or second pluralities of 8-bit data elements" is described at Figures 47D and 47E, and paragraphs 0297.

Regarding claim 39, the recited claim feature "wherein the destination register is a 128-bit register" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 40, the recited claim feature "wherein each of the equal-sized selectors stored in partitioned fields of the index register is a 4-bit selector" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 41, a device having installed therein a programmable processor, the programmable processor comprising in part "an instruction path; a data path; a plurality of registers operable to receive and store data from the data path and communicate the stored data to the data path; and an execution unit coupled to the instruction path and the data path and operable to decode and execute instructions received from the instruction path" is described at Figure 1 and paragraphs 0078-0079.

Regarding claim 41, the recited device having installed therein a programmable processor, the programmable processor further comprising in part an execution unit "wherein in response to decoding a single instruction specifying a plurality of registers storing a plurality of 8-bit data elements, an index register storing an index vector comprising a plurality of equal-sized selectors stored in partitioned fields of the index register and a destination register, the execution unit is operable to, for each selector in the index vector, provide a data element selected by the selector to a predetermined position in the destination register" is described at Figures 1, 47D, and 47E, and paragraphs 0078-0079, 0081, and 0297.

Regarding claim 42, the recited claim feature "wherein the plurality of registers comprises two registers" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 43, the recited claim feature "wherein the plurality of registers comprises two 64-bit registers storing a combined total of sixteen 8-bit data elements" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 44, the recited claim feature "wherein the number of selectors stored in the index register is equal to the number of predetermined positions in the destination register" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 45, the recited claim feature "wherein the index register is a 64-bit register" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 46, the recited claim feature "wherein the index vector comprises n equal-sized selectors and the destination register comprises n equal-sized predetermined positions" is described at Figures 47D and 47E, and paragraphs 0297.

Regarding claim 47, the recited claim feature "wherein the selector stored in a lowest order set of bits of the index register provides a data element to a lowest order set of bits of the destination register, the selector in a second lowest order set of bits of the index register provide a data element to a second lowest order set of bits of the destination register and the selector stored in a highest order set of bits of the index register provides a data element to a highest order set of bits of the destination register" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 48, the recited claim feature "wherein the destination register is a 128-bit register" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 49, the recited claim feature "wherein each of the equal-sized selectors stored in partitioned fields of the index register is a 4-bit selector" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 50, the recited claim feature "wherein the index register stores sixteen 4-bit selectors" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 51, a device having installed therein a programmable processor, the programmable processor comprising in part "an instruction path; a data path; an external interface operable to receive data from an external source and communicate the received data over the data path; a cache operable to retain data communicated between the external interface and the data path; a plurality of registers operable to receive and store data from the data path and communicate the stored data to the data path; and an execution unit coupled to the instruction path and the data path and operable to decode and execute instructions received from the instruction path" is described at Figure 1 and paragraphs 0078-0079.

Regarding claim 51, the recited device having installed therein a programmable processor, the programmable processor further comprising in part an execution unit "wherein in response to decoding a single instruction specifying a first register storing a first plurality of 8-bit data elements, a second register storing a second plurality of 8-bit data elements, an index register storing an index vector comprising a plurality of equal-sized selectors stored in partitioned fields of the index register and a destination register, the execution unit is operable to, for each selector in the index vector, provide a data element from one of the first or second plurality of 8-bit data elements selected by the selector to a predetermined 8-bit position in the destination register, wherein the predetermined positions are contiguous blocks of bits that take up an entire width of the destination register" is described at Figures 1, 47D, and 47E, and paragraphs 0078-0079, 0081, and 0297.

Regarding claim 52, the recited claim feature "wherein the first and second registers are 64-bit registers, the index register is a 64-bit register and each selector stored in the index register has a sufficient number of bits to select anyone of the 8-bit data elements in the first or

second pluralities of 8-bit data elements" is described at Figures 47D and 47E, and paragraphs 0297.

Regarding claim 53, the recited claim feature "wherein the destination register is a 128-bit register" is described at Figures 47D and 47E, and paragraph 0297.

Regarding claim 54, the recited claim feature "wherein each of the equal-sized selectors stored in partitioned fields of the index register is a 4-bit selector" is described at Figures 47D and 47E, and paragraph 0297.

CONCLUSION

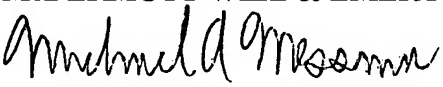
In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Michael A. Messina
Registration No. 33,424

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MAM:DAB
Facsimile: 202.756.8087
Date: November 21, 2006

Please recognize our Customer No. 20277 as our correspondence address.